CLAIMS:

1. An integrated circuit used in an audio playback device, the integrated circuit comprising:

a host interface;

a processing module operably coupled to the host interface;

a multimedia module operably coupled to the processing module;

memory operably coupled to the processing module and to the multimedia module in which digital audio information is stored; and

a filter co-processor operably coupled to the processing module and to the memory, wherein at the direction of the processing module the filter co-processor retrieves digital audio information from the memory and filters the digital audio information.

2. The integrated circuit of claim 1, wherein the filter co-processor comprises:

a plurality of programmable registers operably coupled to the processing module;

a Direct Memory Access (DMA) engine operably coupled to the memory and to the plurality of programmable registers;

a plurality of coefficient register files operably coupled to the DMA engine;

a plurality of sample register files operably coupled to the DMA engine;

a Multiply Accumulator (MAC) engine operably coupled to the plurality of programmable registers, the plurality of coefficient register files, and the plurality of register files; and

an accumulator operably coupled to the MAC engine and to the DMA engine.

3. The integrated circuit of claim 1, wherein when the integrated circuit operates in a playback mode:

the filter co-processor, at the direction of the processing module, retrieves the digital audio information from the memory, filters the digital audio information to produce filtered digital audio information and writes the filtered digital audio information to the memory; and

the multimedia module receives the filtered digital audio information from memory and converts the filtered digital audio information to a playback format.

4. The integrated circuit of claim 3, wherein the filter co-processor performs interpolation filtering on the digital audio information to produce the filtered digital audio information.

5. The integrated circuit of claim 3, wherein the filter co-processor performs graphic equalization filtering on the digital audio information to produce the filtered digital audio information.

6. The integrated circuit of claim 5, wherein in performing graphic equalization filtering on the digital audio information, the filter co-processor performs one of subtractive graphic equalizer filtering in a cascade mode or additive graphic equalizer filtering in a parallel mode.

7. The integrated circuit of claim 1, wherein when the integrated circuit operates in a recording mode:

the multimedia module receives incoming audio information, converts the incoming audio information to incoming digital audio information, and writes the incoming digital audio information to memory; and

the filter co-processor, at the direction of the processing module, retrieves the incoming digital audio information from the memory, filters the incoming digital audio information to produce filtered incoming digital audio information and writes the filtered incoming digital audio information to the memory.

8. The integrated circuit of claim 7, wherein the filter co-processor performs decimation filtering on the incoming digital audio information to produce the filtered incoming digital audio information.

9. The integrated circuit of claim 1, further comprising clock control circuitry that varies the frequency of a clock provided to the filter co-processor to thereby adjust the rate at which the filter-co-processor filters the digital audio information.

10. The integrated circuit of claim 9, wherein:

the clock is also provided to the processing module; and

the clock control circuitry also varies the frequency of the clock provided to the processing module.

11. The integrated circuit of claim 1, further comprising voltage control circuitry that varies a supply voltage provided to the filter co-processor.

12. The integrated circuit of claim 11, wherein the voltage control circuitry also provides and varies the supply voltage provided to the filter co-processor.

13. The integrated circuit of claim 1, wherein in a context switch operation, the filter co-processor receives a context switch operation from the processing module, ceases its current filtering operations, and initiates differing filtering operations.

14. The integrated circuit of claim 13, wherein in the context switch operation, the filter co-processor saves a state of the current filtering operations to memory.

15. A method for operating an audio playback device comprising:

receiving digital audio information via a host interface;

storing the digital audio information in memory;

directing, by a processing module, a filter co-processor to perform filtering operations;

retrieving, by the filter co-processor, the digital audio information from the memory;

filtering, by the filter co-processor, the digital audio information to produce filtered digital audio information; and

storing the filtered digital audio information in the memory.

16. The method of claim 15, further comprising operating in a playback mode by:

retrieving the filtered digital audio information from the memory; and

converting the filtered digital audio information to a playback format.

17. The method of claim 16, wherein the filtering, by the filter co-processor, on the digital audio information to produce the filtered digital audio information comprises interpolation filtering.

18. The method of claim 16, wherein the filtering, by the filter co-processor, on the digital audio information to produce the filtered digital audio information comprises graphic equalizer filtering.

19. The method of claim 18, wherein graphic equalizer filtering includes one of subtractive graphic equalizer filtering in a cascade mode or additive graphic equalizer filtering in a parallel mode.

20. The method of claim 15, further comprising operating in a recording mode b:

receiving incoming audio information;

converts the incoming audio information to incoming digital audio information;

writing the incoming digital audio information to memory;

retrieving, by the filter co-processor, the incoming digital audio information from the memory;

filtering, by the filter co-processor, the incoming digital audio information to produce filtered incoming digital audio information; and

writing, by the filter co-processor, the filtered incoming digital audio information to the memory.

21. The method of claim 20, wherein filtering, by the filter co-processor, comprises decimation filtering on the incoming digital audio information to produce the filtered incoming digital audio information.

22. The method of claim 15, further comprising varying the frequency of a clock provided to the filter co-processor to thereby adjust the rate at which the filter-co-processor filters the digital audio information.

23. The method of claim 22, further comprising varying a supply voltage provided to the filter co-processor.

24. The method of claim 15, further comprising performing a context switch by ceasing ongoing filtering operations of the filter co-processor and initiating differing filtering operations of the filter co-processor.

25. The method of claim 25, further comprising saving a state of the current filtering operations to memory when performing the context switch.

26. An integrated circuit used in an audio playback device, the integrated circuit comprising:

means for receiving digital audio information via a host interface;

means for storing the digital audio information in memory;

means for directing, by a processing module, a filter co-processor to perform filtering operations;

means for retrieving, by the filter co-processor, the digital audio information from the memory;

means for filtering, by the filter co-processor, the digital audio information to produce filtered digital audio information; and

means for storing the filtered digital audio information in the memory.